

Monolithic Digital Stereo FM Transmitter
Radio-Station-on-a-Chip™

KT0803L

▪ Features

Hardware compatible with KT0803K and KT0803M
Additional features to KT0803K and KT0803M
- **Software standby;**
- **Automatic power down power amplifier when silence is detected;**
- **Multiple reference clock support including from 32.768KHz to 26MHz;**
- **ALC (Automatic Level Control)**
- **Higher SNR (Stereo: 66dB)**
- **Increased audio frequency response**
- **Software controlled XTAL selection**

Professional Grade Performance:
- **SNR ≥ 66 dB**
- **Stereo Separation > 40 dB**
- **International compatible 70MHz ~ 108MHz**

Ultra-Low Power Consumption:
- **< 17 mA operation current**
- **< 3 μA standby current**

Simple Interface:
- **Single power supply**
- **Standard 2-wire I^2C MCU interface**

Advanced Digital Audio Signal Processing:
- **On-chip 20-bit ΔΣ Audio ADC**
- **On-chip DSP core**
- **On-chip 24dB PGA with optional 1dB step**
- **Automatic calibration against process and temperature**

1.6V ~ 3.6V supply
Programmable transmit level
Programmable pre-emphasis (50/75 μs)
Pb-free and RoHS Compliant
SOP-16 package

Applications

MP3 Player, Cellular Phone, PDA, PND,
Portable Personal Media player and its accessory,
Laptop Computer, Wireless Speaker

Rev. 1.3

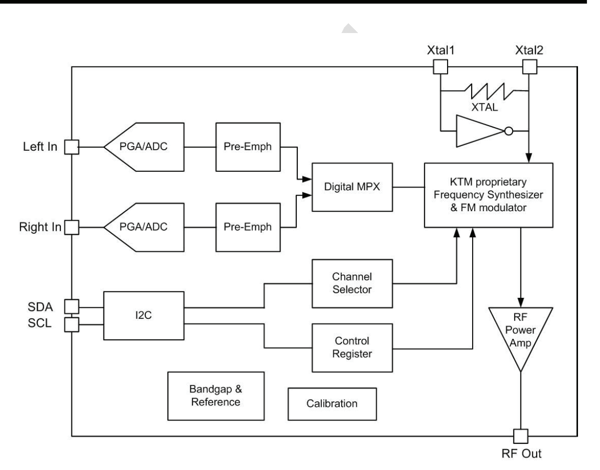


Figure 1: KT0803L System Diagram

▪ General Description

KT0803L, our new generation of low cost Monolithic Digital FM Transmitter, is designed to process high-fidelity stereo audio signal and transmit modulated FM signal over a short range. It's based on the architecture of award-winning KT0801 and it's also an upgrade of KT0803K and KT0803M. The additional features added to KT0803L are standby mode through software, ALC(automatic level control), multiple reference clock, increased SNR performance and frequency response.

The KT0803L features dual 20-bit ΔΣ audio ADCs, a high-fidelity digital stereo audio processor and a fully integrated radio frequency (RF) transmitter. An on-chip low-drop-out regulator (LDO) allows the chip to be integrated in a wide range of low-voltage battery-operated systems with power supply ranging from 1.6V to 3.6V.

The KT0803L is configured as an I^2C slave and programmed through the industry standard 2-wire MCU interface.

Thanks to its high integration level, the KT0803L is mounted in a generic 16-pin SOP package. It only requires a single low-voltage supply. No external tuning is required that makes design-in effort minimum.

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1 Operation Condition

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
1.8V Analog Supply[1]	VDD	Relative to GND	1.6	1.8	2.0	V
IO/Regulator Supply	IOVDD	Relative to GND	1.6		3.6	V
Operating Temp	T_A	Ambient Temperature	0	25	70	°C
Note: 1. No external voltage should be applied to this supply. Decoupling cap should be used instead						

2 Specifications and Features

Table 2: FM Transmitter Functional Parameters (Unless otherwise noted TA = 0-70 °C, IOVDD=1.6~3.6 V, F_{in} = 1 kHz)

Parameter	Symbol	Test/Operating Condition	Min	Nom	Max	Units
FM Frequency Range	F_{tx}	Pin 16	70		108	MHz
Current Consumption	I_{VDD}	Pin 4 with PA (power amp.) at **default power mode (PA_bias = 0, RFGAIN[3:0]=1111)**	-	17		mA
Standby Current	I_{stand}	Pin 4	-	0.1	1	µA
Signal to Noise Ratio	SNR	V_{in} = 1 V_{p-p}, G_{in} = 0	-	66	-	dB
Total Harmonic Distortion	THD	V_{in} = 1 V_{p-p}, G_{in} = 0	-	0.3		%
Left/Right Channel Balance	BAL	V_{in} = 1 V_{p-p}, G_{in} = 0	-0.2	-	0.2	dB
Stereo Separation (Left<->Right)	SEP	V_{in} = 1 V_{p-p}, G_{in} = 0		40	-	dB
Sub Carrier Rejection Ratio	SCR	V_{in} = 1 V_{p-p}, G_{in} = 0	-	-	60	dB
Input Swing[1]	V_{in}	Single-ended input	-	0.35	2	V_{RMS}
PGA Range for Audio Input	G_{in}		-15	0	12	dB
PGA Gain Step for Audio Input	G_{step}		1		4	dB
Required Input Common-Mode Voltage when DC-coupled	V_{cm}	Pin 6,7	0	0.8	1.8	V
Power Supply Rejection[2]	PSRR	IOVDD = 1.9 ~ 3.6 V	40	-	-	dB
Ground Bounce Rejection[2]	GSRR	IOVDD = 1.9 ~ 3.6 V	40	-	-	dB
Input Resistance (Audio Input)	R_{in}	Pin 6, 7	120	150	180	kΩ
Input Capacitance (Audio Input)	C_{in}	Pin 6, 7	0.5	0.8	1.2	pF
Audio Input Frequency Band	F_{in}	Pin 6, 7	20	-	15k	Hz
Transmit Level	V_{out}		96	103	113	dBµV
Channel Step	STEP		-	50		kHz
Pilot Deviation				7.5	15	kHz
Audio Deviation			75		112.5	kHz
Frequency Response		Mono,-3dB, ΔF=60kHz, 50/75µs pre-emphasis	30		15k	Hz
Pre-emphasis Time Constant	T_{pre}	PHTCNST = 1	-	50	-	µs
		PHTCNST = 0	-	75	-	µs
Crystal/External Clock	CLK	Input clock	32.768		40,000	KHz
2-wire I^2C Clock	SCL	Pin 14	0	100	400	kHz
High Level Input Voltage	V_{IH}	Pin 8, 9, 10, 13, 14	0.75 x IOVDD	-	IOVDD + 0.25	V
Low Level Input Voltage	V_{IL}	Pin 8, 9, 10, 13, 14	- 0.25	-	0.25 x IOVDD	V

Notes:
1. Maximum is given on the condition of PGA gain = -15dB.
2. Fin = 20 ~ 15k Hz.

3 Package and Pin List

Table 3: KT0803L Pin Definition

Pin Index	Name	I/O Type	Function
1,5,11,12,15	GND	Ground	Ground
2	XO	Analog I/O	Crystal output.
3	XI/RCLK	Analog I/O	Crystal input or external reference clock input.
4	IOVDD	Power	1.6~3.3V external logic IOVDD
6	INL	Analog Input	Left channel audio input.
7	INR	Analog Input	Right channel audio input.
8	SW1	Digital Input	Control bit. Chip enable, supply mode and crystal selection., see Table 5
9	SW2	Digital Input	
10	RSTB	Digital Input	Reset (active low).
13	SDA	Digital I/O	Serial data I/O.(Integrated 47k ohm pull up resistor)
14	SCL	Digital I/O	Serial clock input. (Integrated 47k ohm pull up resistor)
16	PA_OUT	Analog Output	FM RF output.

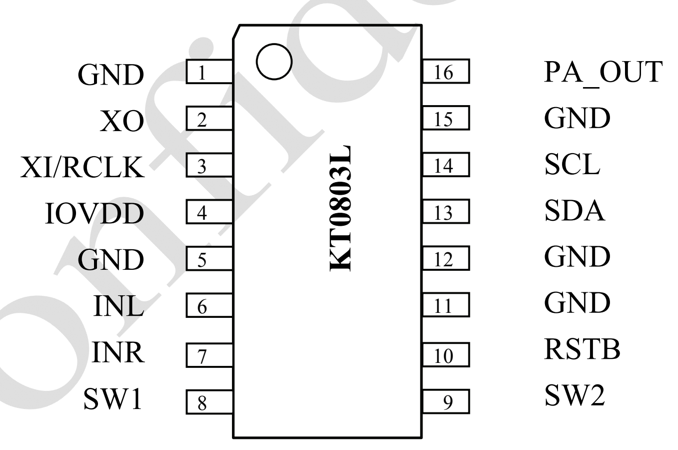


Figure 2: KT0803L Pin-out

I2C Compatible 2-Wire Serial Interface

3.1 General Descriptions

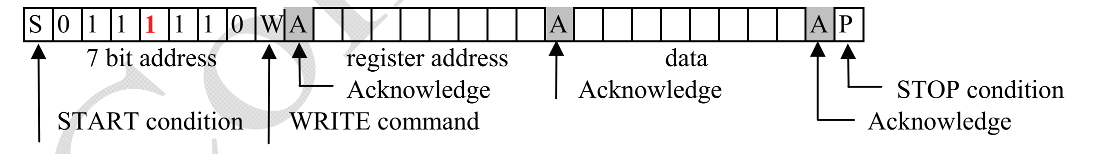
The serial interface consists of a serial controller and registers. An internal address decoder transfers the content of the data into appropriate registers. **Please note that the I2C address is 0x 0111110 the same as in KT0803K and KT0803M. Neither software nor hardware change is needed if KT0803L is used to replace KT0803K and KT0803M.**

Both the write and read operations are supported according to the following protocol:

Write Operations:
BYTE WRITE:
The write operation is accomplished via a 3-byte sequence:
Serial address with write command
Register address
Register data
A write operation requires an 8-bit register address following the device address word and acknowledgment. Upon receipt of this address, the KT0803L will again respond with a "0" and then clock in the 8-bit register data. Following receipt of the 8-bit register data, the KT0803L will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition (see Figure 3).

Read Operations:
RANDOM READ:
The read operation is accomplished via a 4-byte sequence:
Serial address with write command
Register address
Serial address with read command
Register data
Once the device address and register address are clocked in and acknowledged by the KT0803L, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The KT0803L acknowledges the device address and serially clocks out the register data. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 3).

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE

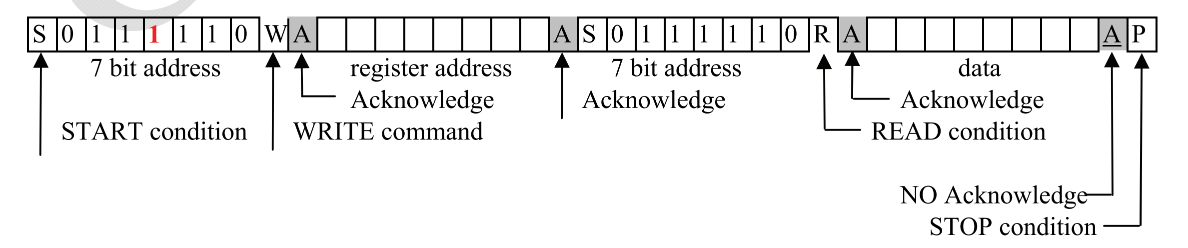


Figure 3: Serial Interface Protocol

CURRENT ADDRESS READ: The internal data register address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the KT0803L, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 4).

CURRENT REGISTER READ PROCEDURE

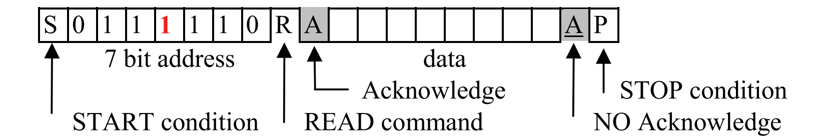


Figure 4: Serial Interface Protocol

Note: The serial controller supports slave mode only. Any register can be addressed randomly.

The address of the slave in the first 7 bits and the 8th bit tells whether the master is receiving data from the slave or transmitting data to the slave. The I^2C write address is 0x7C and the read address is 0x7D.

3.2 Slave Mode Protocol

With reference to the clocking scheme shown in Figure 5, the serial interface operates in the following manner:



Figure 5: Serial Interface Slave Mode Protocol

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 6). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 7).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the KT0803L in a standby power mode (see Figure 7).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the KT0803L in 8-bit words. The KT0803L sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle (see Figure 8).



Data Validity

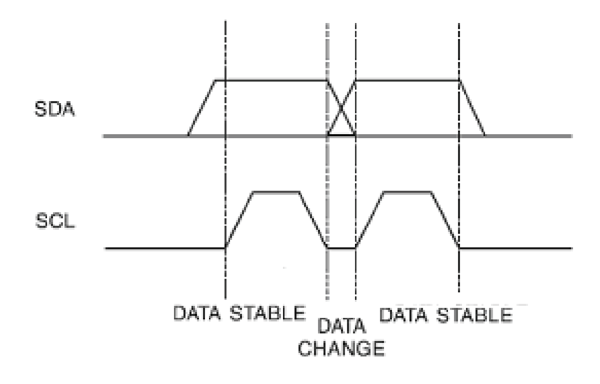


Figure 6: Clock and Data Transitions

Start and Stop Definition

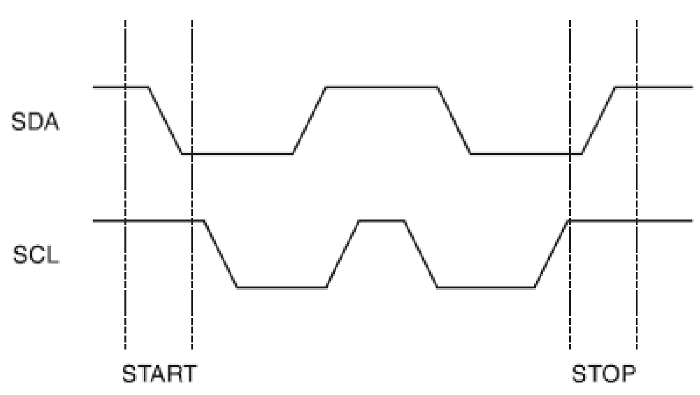


Figure 7: Start and Stop Definition

Output Acknowledge

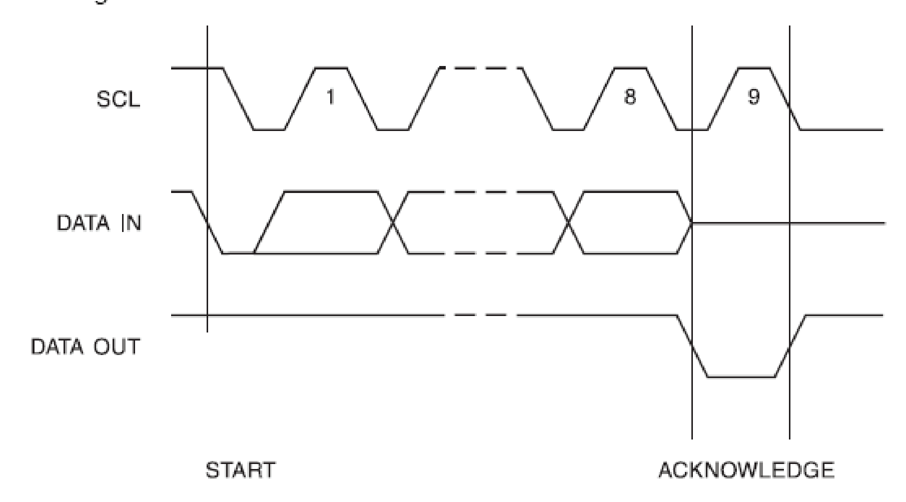


Figure 8: Acknowledge

4 Register Bank

The register bank stores channel frequency codes, calibration parameters, operation status, mode and power controls, which can be accessed by the internal digital controller, state machines and external micro controllers through the serial interface.

All registers are 8 bits wide. Control logics are active high unless specifically noted.

Register	7	6	5	4	3	2	1	0
0x00	CHSEL[8:1]							
0x01	RFGAIN[1:0]		PGA[2:0]			CHSEL[11:9]		
0x02	CHSEL[0]	RFGAIN[3]	-	-	MUTE	PLTADJ	-	PHTCNST
0x04	ALC_EN	MONO	PGA_LSB[1:0]		-		BASS[1:0]	
0x0B	Standby	-	PDPA	-	-	AUTO_PADN	-	-
0x0C	ALC_DECAY_TIME[3:0]				ALC_ATTACK_TIME[3:0]			
0x0E	-	-	-	-	-	-	PA_BIAS	-
0x0F	-	-	-	PW_OK	-	SLNCID	-	-
0x10	-	-	-	-		-	-	PGAMOD
0x12	SLNCDIS	SLNCTHL[2:0]			SLNCTHH[2:0]			SW_MOD
0x13	RFGAIN[2]	-	-	-	-	PA_CTRL	-	-
0x14	SLNCTIME[2:0]			SLNCCNTHIGH[2:0]			-	SLNCTIME[3]
0x15	ALCCMPGAIN[2:0]							
0x16	-			-	-	SLNCCNTLOW[2:0]		
0x17	-	FDEV	AU_ENHANCE		XTAL_SEL			
0x1E		DCLK	XTALD		REF_CLK[3:0]			
0x26	ALCHOLD[2:0]				ALCHIGHTH[2:0]			
0x27					ALCLOWTH[3:0]			

Note 1: ONLY read/write the defined registers.

Note 2: Shaded registers are new or changed in KT0803L.

4.1 Register 0x00 (Address: 0x00, Default value: 0x5C)

Bit	7	6	5	4	3	2	1	0
KT0803L	CHSEL[8:1]							

Please note that the default channel of KT0803L is 86MHz instead of 89.7MHz in KT0803K and KT0803M.

CHSEL[11:0] = Dec2Bin (Target frequency in MHz x 20),

where CHSEL[11:0] = Reg0x1[2:0]:Reg0x0[7:0]:Reg0x2[7]

4.2 Register 0x01 (Address: 0x01, Default value: 0xC3)

Bit	7	6	5	4	3	2	1	0
KT0803L	RFGAIN[1:0]		PGA[2:0]			CHSEL[11:9]		

Bits	Type	Default	Label	Description
7:6	RW	11	RFGAIN[1:0]	Transmission Range Adjustment with RFGAIN[3] in Reg 0x02[6] and RFGAIN[2] in Reg 0x13[7] (See Table 4 below)

Bits	Type	Default	Label	Description
5:3	RW	000	PGA[2:0]	PGA Gain Control (see PGA_LSB description, Reg 0x04) 111: 12dB 110: 8dB 101: 4dB 100: 0dB 000: 0dB 001: -4dB 010: -8dB 011: -12dB
2:0	RW	011	CHSEL[11:9]	FM Channel Selection[11:9]

Table 4: Transmission power setting

RFGAIN[3:0]	RFOUT
0000	95.5 dBuV
0001	96.5 dBuV
0010	97.5 dBuV
0011	98.2 dBuV
0100	98.9 dBuV
0101	100 dBuV
0110	101.5 dBuV
0111	102.8 dBuV
1000	105.1 dBuV (107.2dBuV PA_BIAS=1)
1001	105.6 dBuV (108dBuV, PA_BIAS=1)
1010	106.2 dBuV (108.7dBuV, PA_BIAS=1)
1011	106.5 dBuV (109.5dBuV, PA_BIAS=1)
1100	107 dBuV (110.3dBuV, PA_BIAS=1)
1101	107.4 dBuV (111dBuV, PA_BIAS=1)
1110	107.7 dBuV (111.7dBuV, PA_BIAS=1)
1111 (default setting)	108 dBuV (**112.5dBuV, PA_BIAS=1**)

4.3 Register 0x02 (Address: 0x02, Default: 0x40)

Bit	7	6	5	4	3	2	1	0
KT0803L	CHSEL[0]	RFGAIN[3]	-	-	MUTE	PLTADJ	-	PHTCNST

Bits	Type	Default	Label	Description
7	RW	0	CHSEL[0]	LSB of CHSEL
6	RW	1	RFGAIN[3]	MSB of RFGAIN
5:4	RW	00	Reserved	Reserved
3	RW	0	MUTE	Software Mute 0: MUTE Disabled 1: MUTE Enabled
2	RW	0	PLTADJ	Pilot Tone Amplitude Adjustment 0: Amplitude low 1: Amplitude high
1	RW	0	Reserved	Reserved
0	RW	0	PHTCNST	Pre-emphasis Time-Constant Set 0: 75 μs (USA, Japan) 1: 50 μs (Europe, Australia)

4.4 Register 0x04 (Address: 0x04, Default: 0x04)

Bit	7	6	5	4	3	2	1	0
KT0803L	ALC_EN	MONO	PGA_LSB[1:0]		-		BASS[1:0]	
KT0803K/M	-	MONO	PGA_LSB[1:0]		FDEV[1:0]		BASS[1:0]	

Bits	Type	Default	Label	Description
7	RW	0	ALC_EN	Automatic Level Control Enable Control 0 = Disable ALC 1 = Enable ALC
6	RW	0	MONO	0 = Stereo 1 = Mono
5:4	RW	00	PGA_LSB[1:0]	

PGA[2:0]	PGA_LSB[1:0]	PGA Gain
111	**11**	**12dB**
111	10	11
111	01	10
111	00	9
110	**11**	**8**
110	10	7
110	01	6
110	00	5
101	**11**	**4**
101	10	3
101	01	2
101	00	1
100	**11**	**0**
100	10	0
100	01	0
100	00	0
000	**00**	**0**
000	01	-1
000	10	-2
000	11	-3
001	**00**	**-4**
001	01	-5
001	10	-6
001	11	-7
010	**00**	**-8**
010	01	-9
010	10	-10
010	11	-11
011	**00**	**-12**
011	01	-13
011	10	-14
011	11	-15

Bits	Type	Default	Label	Description
3:2	RW	01	Reserved	Reserved
1:0	RW	00	BASS[1:0]	Bass Boost Control 00 : Disabled 01 : 5dB 10 : 11dB 11 : 17dB

4.5 Register 0x0B (Address: 0x0B, Default: 0x00)

Bit	7	6	5	4	3	2	1	0
KT0803L	Standby	-	PDPA	-	-	AUTO_PADN	-	-
KT0803K/M	-	-	PDPA	-	-	-	-	-

Bits	Type	Default	Label	Description
7	RW	0	Standby	Chip Standby Control Bit 0 = Normal operation 1 = Standby enable
6	RW	0	Reserved	Reserved
5	RW	0	PDPA	Power Amplifier Power Down 0 = Power amplifier power on 1 = Power amplifier power down
4	RW	0	Reserved	Reserved
3	RW	0	Reserved	Reserved
2	RW	0	AUTO_PADN	Automatic Power Down Power Amplifier When Silence is Detected 0 = Disable this feature 1 = Enable this feature
1	RW	0	Reserved	Reserved
0	RW	0	Reserved	Reserved

4.6 Register 0x0C (Address: 0x0C, Default: 0x00) - New

Bit	7	6	5	4	3	2	1	0
KT0803L	ALC_DECAY_TIME[3:0]				ALC_ATTACK_TIME[3:0]			

Bits	Type	Default	Label	Description
7:4	RW	0000	ALC_DECAY_TIME[3:0]	ALC Decay Time Selection 0000 = 25us 0001 = 50us 0010 = 75us 0011 = 100us 0100 = 125us 0101 = 150us 0110 = 175us 0111 = 200us 1000 = 50ms 1001 = 100ms 1010 = 150ms 1011 = 200ms 1100 = 250ms 1101 = 300ms 1110 = 350ms 1111 = 400ms

Bits	Type	Default	Label	Description
3:0	RW	0000	ALC_ATTACK_TIME[3:0]	ALC Attack Time Selection 0000 = 25us 0001 = 50us 0010 = 75us 0011 = 100us 0100 = 125us 0101 = 150us 0110 = 175us 0111 = 200us 1000 = 50ms 1001 = 100ms 1010 = 150ms 1011 = 200ms 1100 = 250ms 1101 = 300ms 1110 = 350ms 1111 = 400ms

4.7 Register 0x0E (Address: 0x0E, Default: 0x02)

Bit	7	6	5	4	3	2	1	0
KT0803L	-	-	-	-	-	-	PA_BIAS	-

Bits	Type	Default	Label	Description
7:2	RW	0x00	Reserved	Reserved
1	RW	1	PA_BIAS	PA Bias Current Enhancement. 0 = Disable PA bias 1 = Enable PA bias
0	RW	0	Reserved	Reserved

4.8 Register 0x0F (Address: 0x0F, Read only)

Bit	7	6	5	4	3	2	1	0
KT0803L	-	-	-	PW_OK	-	SLNCID	-	-

Bits	Type	Default	Label	Description
7	R	NA	Reserved	Reserved
6	R	NA	Reserved	Reserved
5	R	NA	Reserved	Reserved
4	R	NA	PW_OK	Power OK Indicator
3	R	NA	Reserved	Reserved
2	R	NA	SLNCID	1 when Silence is Detected
1	R	NA	Reserved	Reserved
0	R	NA	Reserved	Reserved

4.9 Register 0x10 (Address: 0x10, Default: 0xA8)

Bit	7	6	5	4	3	2	1	0
KT0803L	-	-	-	-	-	-	-	PGAMOD
KT0803K/M	-	-	-	LMTLVL[1:0]		-	-	PGAMOD

Bits	Type	Default	Label	Description
7:5	RW	101	Reserved	Reserved
4:3	RW	01	Reserved	Reserved
2:1	RW	00	Reserved	Reserved
0	RW	0	PGAMOD	PGA Mode Selection 0 = 4dB step 1 = 1dB step with PGA_LSB[1:0] used

4.10 Register 0x12 (Address: 0x12, Default: 0x80)

Bit	7	6	5	4	3	2	1	0
KT0803L	SLNCDIS	SLNCTHL[2:0]			SLNCTHH[2:0]			SW_MOD

Bits	Type	Default	Label	Description
7	RW	1	SLNCDIS	Silence Detection Disable 0 : Enable 1 : Disable
6:4	RW	000	SLNCTHL	Silence Detection Low Threshold 000 : 0.25mv 001 : 0.5mv 010 : 1mv 011 : 2mv 100 : 4mv 101 : 8mv 110 : 16mv 111 : 32mv
3:1	RW	000	SLNCTHH	Silence Detection High Threshold 000 : 0.5mv 001 : 1mv 010 : 2mv 011 : 4mv 100 : 8mv 101 : 16mv 110 : 32mv 111 : 64mv
0	RW	0	SW_MOD	Switching Channel Mode Selection. 0 = Mute when changing channel 1 = PA off when changing channel

4.11 Register 0x13 (Address: 0x13, Default: 0x80)

Bit	7	6	5	4	3	2	1	0
KT0803L	RFGAIN[2]	-			-	PA_CTRL	-	-

Bits	Type	Default	Label	Description
7	RW	1	RFGAIN[2]	PA (Power amplifier) power (combined with Reg 0x01[7:6] and Reg 0x02[6])to set up transmission range)
6:3	RW	0000	Reserved	Reserved

Bits	Type	Default	Label	Description
2	RW	0	PA_CTRL	**Power amplifier structure selection** 0 = Internal power supply, KT0803 compatible 1 = External power supply via external inductor **Note : When an external inductor is used, this bit must be set to 1 immediately after the Power OK indicator Reg 0x0F[4] is set to 1. Otherwise, the device may be destroyed!**
1:0	RW	00	Reserved	Reserved

4.12 Register 0x14 (Address: 0x14, default 0x00)

Bit	7	6	5	4	3	2	1	0
KT0803L	SLNCTIME[2:0]			SLNCCNTHIGH[2:0]			-	SLNC_TIME[3]
KT0803K/M	SLNCTIME[2:0]			SLNCCNTHIGH[2:0]			-	-

Bits	Type	Default	Label	Description
7:5	RW	000	SLNCTIME[2:0]	Silence Detection Low Level and High Level Duration Time 000 : 50ms (16s if SLNCTIME[3] = 1) 001 : 100ms (24s if SLNCTIME[3] = 1) 010 : 200ms (32s if SLNCTIME[3] = 1) 011 : 400ms (40s if SLNCTIME[3] = 1) 100 : 1s (48s if SLNCTIME[3] = 1) 101 : 2s (56s if SLNCTIME[3] = 1) 110 : 4s (60s if SLNCTIME[3] = 1) 111 : 8s (64s if SLNCTIME[3] = 1)
4:2	RW	000	SLNCCNTHIGH[2:0]	Silence Detection High Level Counter Threshold 000 : 15 001 : 31 010 : 63 011 : 127 100 : 255 101 : 511 110 : 1023 111 : 2047
1	RW	0	Reserved	Reserved
0	RW	0	SLNCTIME[3]	Silence Detection Long Duration Time Enable 0 = Short duration time enable 1 = Long duration time enable

4.13 Register 0x15 (Address 0x15, default: 0xE0) - New

Bit	7	6	5	4	3	2	1	0
KT0803L	ALCCMPGAIN[2:0]			-	-	-		

Bits	Type	Default	Label	Description

Bits	Type	Default	Label	Description
7:5	RW	111	ALCCMPGAIN[2:0]	ALC Compressed Gain Setting 100 = 06 (6dB) 101 = 03 (3dB) 110 = 00 (0dB) 111= 1D (-3dB) 000 = 1A(-6dB) 001 = 17(-9dB) 010 = 14(-12dB) 011 = 11(-15dB)
4:0	R		Reserved	Reserved

4.14 Register 0x16 (Address 0x16, default: 0x00)

Bit	7	6	5	4	3	2	1	0
KT0803L	-			-	-	SLNCCNTLOW[2:0]		

Bits	Type	Default	Label	Description
7:3	RW	0x0	Reserved	Reserved
2:0	RW	000	SLNCCNTLOW[2:0]	Silence Low Counter 000 : 1 001 : 2 010 : 4 011 : 8 100 : 16 101 : 32 110 : 64 111 : 128

4.15 Register 0x17 (Address 0x17, default: 0x00) - New

Bit	7	6	5	4	3	2	1	0
KT0803L	-	FDEV	AU_ENHANCE	-	XTAL_SEL			

Bits	Type	Default	Label	Description
7	RW	0	Reserved	Reserved
6	RW	0	FDEV	Frequency Deviation Delection 0 = 75kHz deviation 1 = 112.5kHz deviation
5	RW	0	AU_ENHANCE	Audio Frequency Response Enhancement Enable 0 = Disable 1 = Enable
4	RW	0	Reserved	Reserved
3	RW	0	XTAL_SEL	Software Controlled Crystal Oscillator Selection 0 = 32.768kHz crystal 1 = 7.6MHz crystal

4.16 Register 0x1E (Address 0x1E, default: 0x00) - New

Bit	7	6	5	4	3	2	1	0
KT0803L	-	DCLK	XTALD	-	REF_CLK[3:0]			

Bits	Type	Default	Label	Description
7	RW	0	Reserved	Reserved
6	RW	0	DCLK	Multiple Reference Clock Selection Enable 0 = Disable multiple reference clock feature and reference clock or crystal oscillator can only select through SW1/SW2 pins. 1 = Enable multiple reference clock and user can select different reference clock through REF_CLK[3:0]
5	RW	0	XTALD	Crystal Oscillator Disable Control 0 = Enable crystal oscillator 1 = Disable crystal oscillator
4	RW	0	Reserved	Reserved
3:0	RW	0000	REF_CLK[3:0]	Reference Clock Selection 0000 = 32.768kHz 0001 = 6.5MHz 0010 = 7.6MHz 0011 = 12MHz 0100 = 13MHz 0101 = 15.2MHz 0110 = 19.2MHz 0111 = 24MHz 1000 = 26MHz Others = Reserved

4.17 Register 0x26 (Address 0x26, default: 0xA0) - New

Bit	7	6	5	4	3	2	1	0
KT0803L	ALCHOLD[2:0]			-	ALCHIGHTH[2:0]			-
KT0803K/M	-			-	-			

Bits	Type	Default	Label	Description
7:5	RW	101	ALCHOLD[2:0]	ALC Hold Time Selection 000 = 50ms 001 = 100ms 010 = 150ms 011 = 200ms 100 = 1s 101 = 5s 110 = 10s 111 = 15s
4	RW	0	Reserved	Reserved
3:1	RW	000	ALCHIGHTH[2:0]	ALC High Threshold Selection 000 = 0.6 001 = 0.5 010 = 0.4 011 = 0.3 100 = 0.2 101 = 0.1 110 = 0.05 111 = 0.01
0	RW	0	Reserved	Reserved

4.18 Register 0x27 (Address 0x27, default: 0x00) - New

Bit	7	6	5	4	3	2	1	0
KT0803L	-	-	-	-	ALCLOWTH[3:0]			

Bits	Type	Default	Label	Description
7:4	RW	0000	Reserved	Reserved
3:0	RW	0000	ALCLOWTH[3:0]	ALC Low Threshold 0000 = 0.25 0001 = 0.2 0010 = 0.15 0011 = 0.1 0100 = 0.05 0101 = 0.03 0110 = 0.02 0111 = 0.01 1000 = 0.005 1001 = 0.001 1010 = 0.0005 1011 = 0.0001 Others = Reserved

5 Chip Enable and Mode Control

There are three pins SW1/SW2 to enable the chip and determine the reference clock or crystal. The definition is shown below.

Table 5: Pin SW1/SW2

SW1	SW2	Chip Mode	IOVDD	Clock Source
0	0	Power Off	1.6~3.6V	N/A
0	1	Power On	1.6~3.6V	12MHz
1	0	Power On	1.6~3.6V	32.768KHz
1	1	Power On	1.6~3.6V	7.6MHz

6 Mute

The FM transmitter can be muted by setting Register MUTE to "1" through I2C programming.

7 Silence Detection

Bit name	Register location	Description
SLNCDIS	Reg 0x12[7]	Setting to 0 to enable the silence detection
SLNCTIME[2:0]	Reg 0x14[7:5]	Silence detection time window
SLNCTIME[3]	Reg 0x14[0]	Silence detection long time window
SLNCTHL[2:0]	Reg 0x12[6:4]	Low threshold voltage of input signal for silence detection
SLNCTHH[2:0]	Reg 0x12[3:1]	High threshold voltage of input signal for silence detection
SLNCCNTTHL[2:0]	Reg 0x14[4:2]	# of time when the input signal amplitude is lower than SLNCTHL
SLNCCNTTHH[2:0]	Reg 0x16[2:1]	# of time when the input signal amplitude is higher than SLNCTHH
SLNCID	Reg 0x0F[2]	(Read only) Set to 1 when silence is detected.

The silence detection scheme is enabled by setting SLNCDIS to 0.

During the time defined by SLNTIME[2:0], the chip will be muted when the number of time when the input amplitude is higher than the voltage defined by SLNCTHL[2:0] is lower than SLNCCNTTHL[2:0]. The SLNCID bit is set to 0. In KT0803L, SLNCTIME[3] is added to increase the silence time, which allow user set the silence time up to 64s. Another enhanced feature is that KT0803L can power down power amplifier automatically if the silence time meet the specified value by setting AUTO_PADN to 1.

When the input signal amplitude is higher than the voltage defined by SLNCTHH[2:0] and the number of time when that happens is more than SLNCCNTTHH[2:0], the chip exits from the mute status and the SLNCID is cleared to 0.

8 ALC (Automatic Level Control)

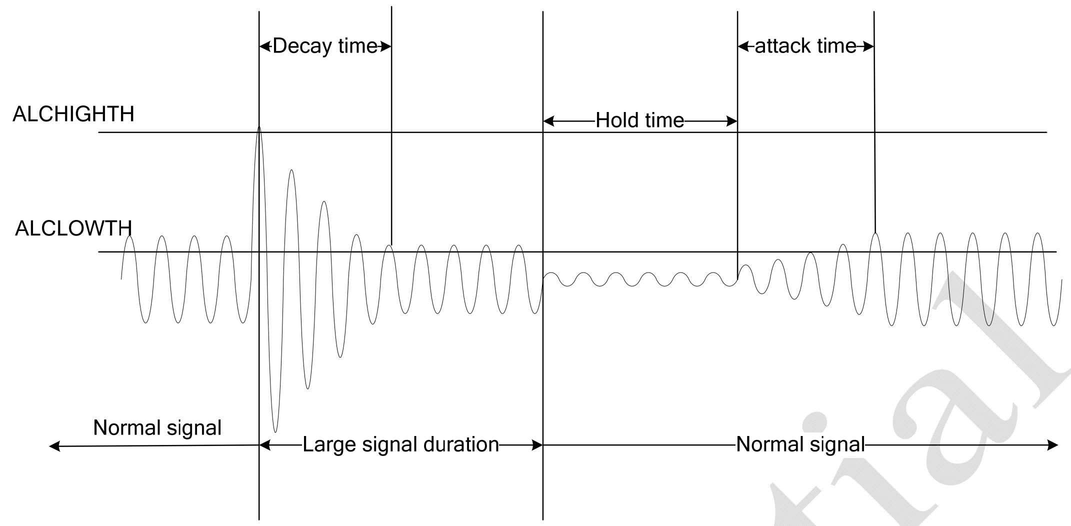


Figure 9 ALC working principle

Bit name	Register location	Description
ALC_DECAY_TIME[3:0]	Reg0x0C[7:4]	ALC decay time
ALC_ATTACK_TIME[3:0]	Reg0x0C[3:0]	ALC attack time
ALCHOLD[2:0]	Reg0x26[7:5]	ALC hold time
ALCHIGHTH[2:0]	Reg0x26[3:1]	ALC high threshold level
ALCLOWTH[3:0]	Reg0x27[3:0]	ALC low threshold level
ALCCMPGAIN	Reg0x15[7:5]	ALC compressed gain
ALC_EN	Reg0x04[7]	ALC enable control

ALC is used to control the audio gain automatically according to the amplitude of the current input signal as shown in Figure 9. Once the signal higher than the value specified in register ALCHIGHTH is detected, the audio gain will be compressed to the value specified in register ALCCMPGAIN automatically. The time used to decrease from current audio gain to compressed audio gain is called decay time and can be specified through register ALC_DECAY_TIME[3:0]. If all the signal level are below the value specified in register ALCLOWTH[3:0] within a certain time(this time is called hold time and can be specified through register ALCHOLD[2:0]), the audio will be increase from the compressed gain to original gain. The gain rising time is called attack time and this time can also be specified in register ALC_ATTACK_TIME[3:0].

9 Reset

The global reset is issued after the RSTB pin set to “0” or automatic on-chip power-on reset. After a global reset, all registers are reset to the default value.

10 Typical Application Circuits

The KT0803L can be integrated in a wide range of systems by requiring only a single power supply.

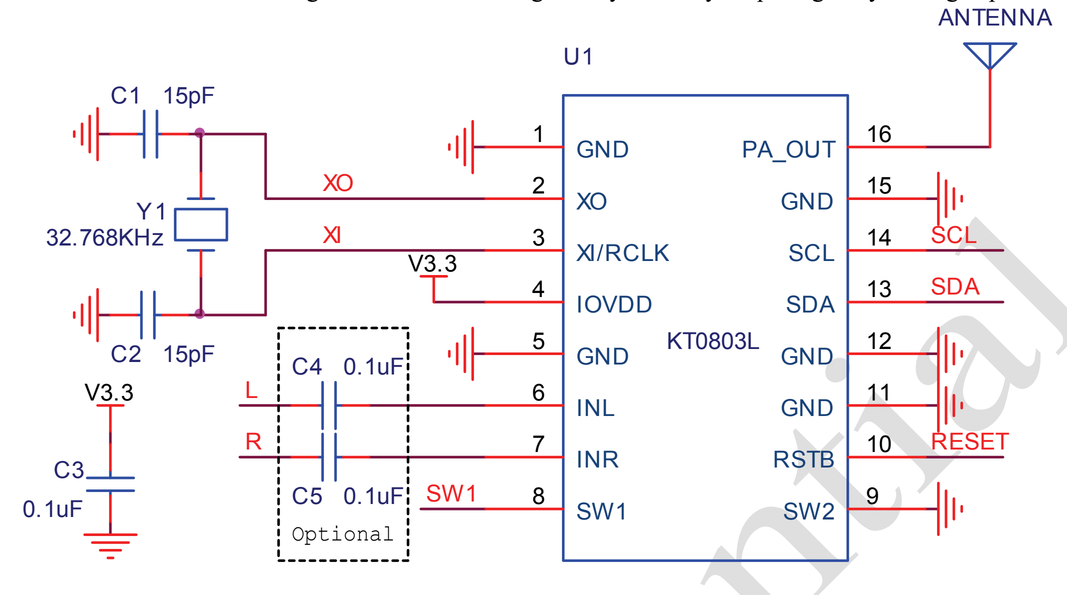


Figure 10 shows the external diagram for the drop-in replacement of KT0803K and KT0803M.

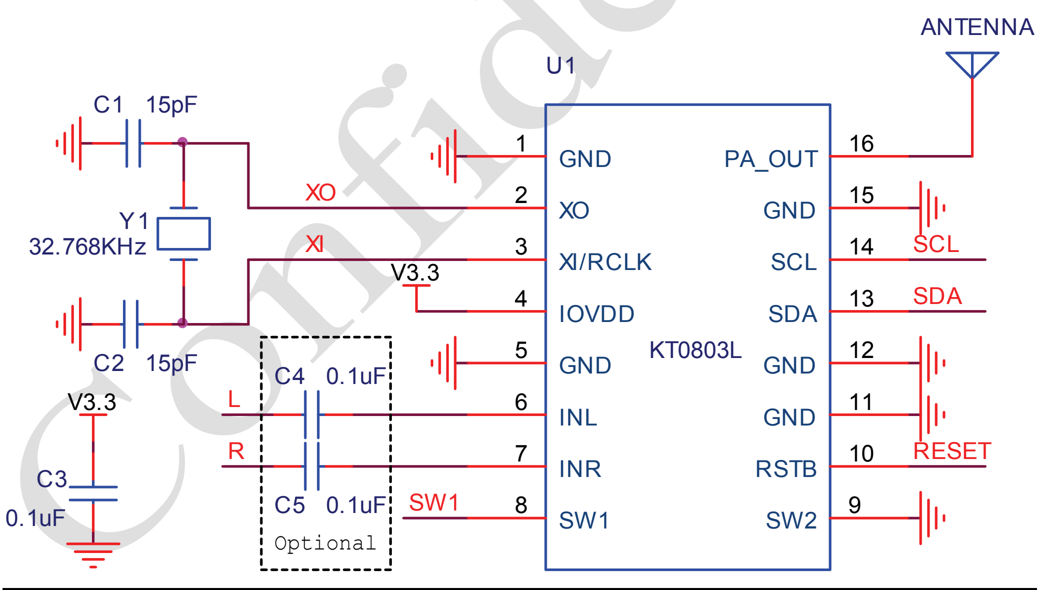


Figure 10: Typical configuration for a drop-in replacement

As shown in the block above, KT0803L is fully compatible with KT0803K and KT0803M

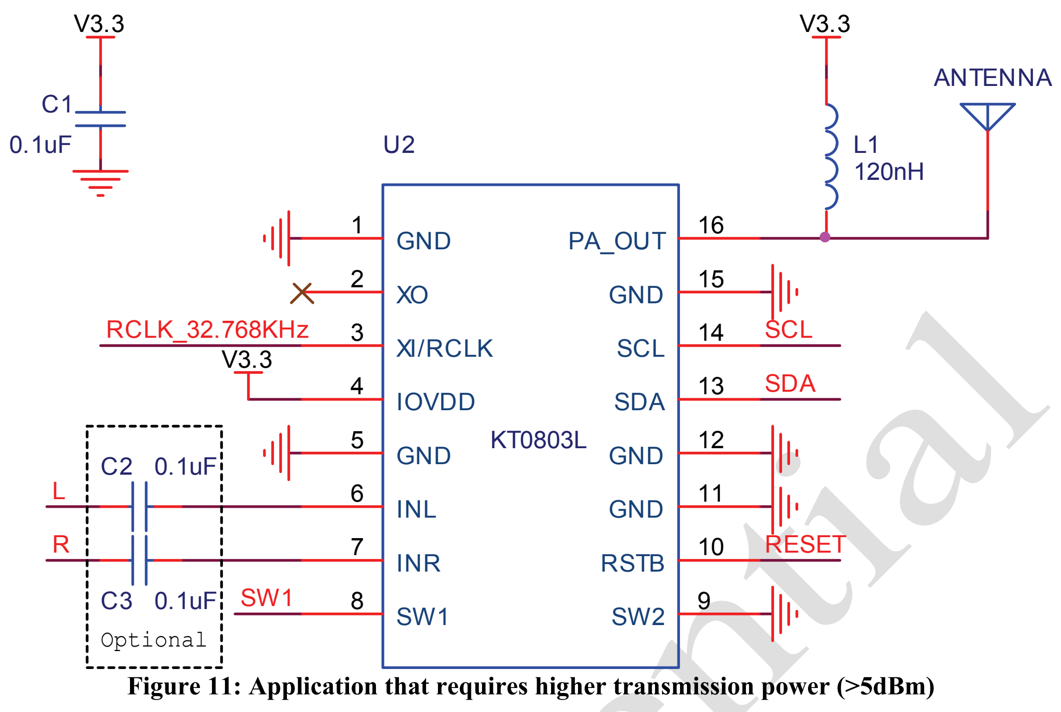
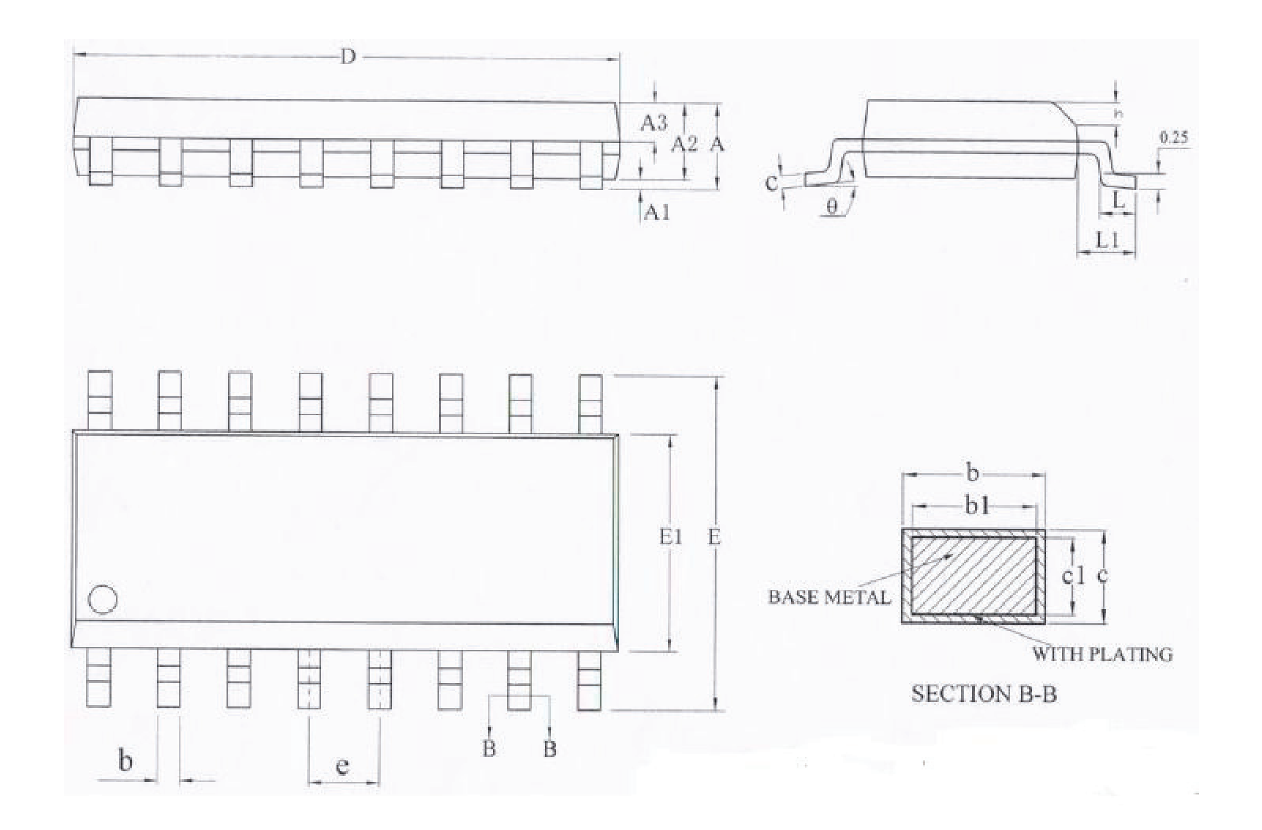


Figure 11: Application that requires higher transmission power (>5dBm)

11 Package Outline



Symbols	(MILLIMETERS)			Symbols	(MILLIMETERS)		
	MIN	NOM	MAX		MIN	NOM	MAX
A			1.75	D	9.70	9.90	10.10
A1	0.10		0.25	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39		0.48	h	0.25		0.50
b1	0.38	0.41	0.43	L	0.50		0.80
c	0.21		0.26	L1		1.05BSC	
C1	0.19	0.20	0.21	θ	0		8°

12 Revision History

V1.0 Official Release
V1.1 Updated application circuits
V1.2 Deleted "HF" pin and fixed the some mistake of test condition in table 2
V1.3 Deleted "GPIO[1:0]" register.
Modified Table 3, Table 5, Figure 10 and Figure 11.

13 Contact Information

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